DIGITAL COMMUNICATIONS SYSTEM

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Abstract

A local area network data communications system of the type providing communication between at least a pair of computer devices interfaced with associated communication nodes (52), said nodes including a transceiver (50, 51) wherein said nodes are commonly connected to a pair of communication lines (53, 54), said lines extending throughout the local area network, said lines carrying transmitted signals, each node being adapted to transmit or receive said data to and from said lines.

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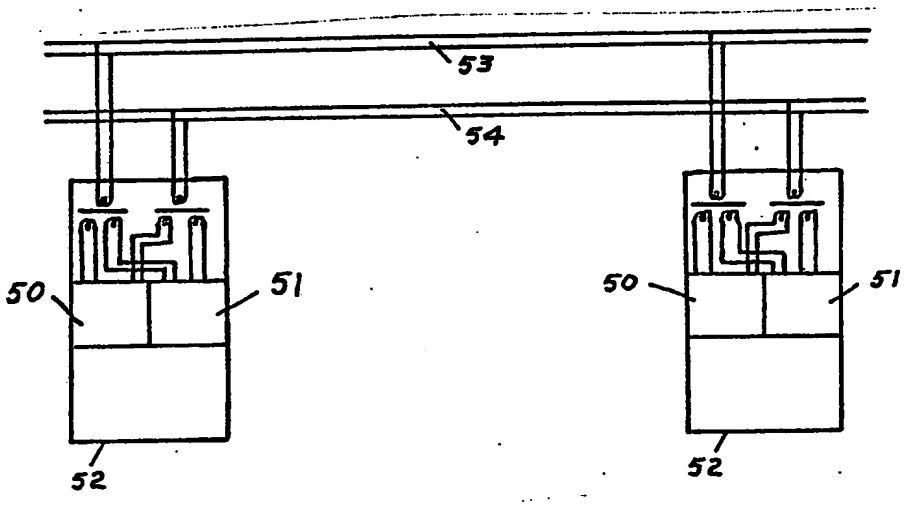

(57) Abstract

A local area network data communications system of the type providing communication between at least a pair of computer devices interfaced with associated communication nodes (52), said nodes including a transceiver (50, 51) wherein said nodes are commonly connected to a pair of communication lines (53, 54), said lines extending throughout the local area network, said lines carrying transmitted signals, each node being adapted to transmit or receive said data to and from said lines.

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DIGITAL COMMUNICATIONS SYSTEM

BACKGROUND OF THE INVENTION

The present invention relates to a system of communication with between at least two computers devices and more particularly a digital data communication system incorporating one or more communication bus adaptors consisting of two or more micro-processors and communication interfaces to the bus pathway and to serial communication lines to terminals, computers and to remote bus adaptors forming part of the other local networks.

In the field of local area computer networks a broad class of networks use a common communication bus to connect several communicating entities called nodes in the manner disclosed in U.S. Patent Specification 4063220 assigned to Xerox Corporation. A feature of such a network is that a message transmitted by any node onto the common bus can be received by every other node. It is necessary to devise a method for regulating and controlling the use of the common bus by competing nodes (bus access method). Many methods have been described for example, token passing method or polling method; the one with which the invention is concerned is a method generally known as the "Carrier-sense Multiple Access with Collision-detection" method, abbreviated to "CSMA-CO". The essential features of CSMA-CO are:

1. Before transmitting, each node monitors the state of the bus. A node begins to transmit only if the bus is sensed to be idle.

2. While transmitting a node tests the signal on the bus to detect interference from other nodes. This can occur if two or more nodes begin transmitting almost simultaneously. When this happens a "collision" is said to have occurred; i.e. two (or more) messages have "collided" on the bus.

3. After a collision all transmitting nodes stop transmitting and a back-off algorithm then determines which

of them should start again. We are not concerned with the details of this algorithm, many of which have been devised.

4. It is possible that another collision will occur on the second atempt to transmit the message. If it does, the nodes stop, back-off, and go through the cycle again. The back-off algorithm must be designed so that the cycle does not repeat continuously.

The Carrier-sense Multiple-access method imposes certain requirements on the encoding and decoding sections of the transmitters and receivers used in the nodes:

1. The receiver must be able to proces both the transmissions from nearby nodes (large signal amplitude), and the most distant nodes on the bus (small signal amplitude); i.e. the receiver is required to have adequate cynamic range.

2. In order to detect collisions the receiver must be able to detect a distant (weak) signal in the presence of a strong signal.

3. It is desirable that the receiver be able to detect unequivocally whether the bus is busy or idle.

OBJECTS OF THE INVENTION

1. A principal objective of the present invention is the simple recovery of a timing reference signal (received clock) in a receiver;

2. The simple and unambiguous recovery of received data;

3. The operation of the receiver is not affected by the polarity of the received signal; (i.e. the two wires of a balanced medium such as a twisted-wire pair can be reversed without affecting the ability of the receiver to operate);

4. Detection of collisions is very fast (within a few bit times), and does not require comparison of transmitted and received signals;

5. To provide a receiver which needs no preamble signal on which to synchronize;

6. Most of the energy in the transmitted signal

is contained in a relatively small bandwidth of frequency. This is important with transmission media such as twisted-wire pairs which are characterized by an attenuation function which increases fairly rapidly with increasing frequency;

7. The transmitted signal has not direct current components. This allows transformer-coupling between the nodes and the bus.

SUMMARY

A local area network data communications system of the type providing communication between at least a pair of computer devices interfaced with associated communication nodes 52, said nodes including a transceiver 50, 51, wherein said nodes are commonly connected to a pair of communication lines 53, 54, said lines extending throughout the local area network, said lines carrying transmitted signals, each node being adapted to transmit or receive said data to and from said lines.

More specifically one communication line carries binary one signals and the other line carried binary zero signals.

In one aspect of the invention the data communication lines include non-interacting twisted wire pairs, as a pair of co-axial or twin-axial cables.

The nodes perform the encoding of benary data into a form suitable for transmitting on the communication lines having equal signal capacity as bandwidth, and the decoding of data received from both lines.

The line coding method of the present invention does not require a "preamble" thus representing a saving in overheads particularly with short messages.

The two communication lines which are preferably balanced such as a twisted wire pair can be reversed without affecting the ability of the receiver or transmitter to operate.

In a further aspect of the invention the nodes include means to detect and signal the existence of

simultaneous signal pulses on both lines thereby indicating a collision, and means to retransmit data after a predetermined delay.

BRIEF DESCRIPTION OF DRAWINGS

Figure 1 is a schematic block diagram showing cable pairs and node connections.

Figures 2 and 4 are a schematic diagram of a transmitter and receiver in a node respectively.

Figures 3 and 5 show pulse diagrams.

DESCRIPTION OF SPECIFIC EMBODIMENT

Each node 52 is connected to non-interacting cables 53 and 54. The cables may be twisted pairs, co- or twin-axial cables.

Each node is controlled by one or more micro processors (not shown) to manage the storage of data in the node, the sequencing of packets of data and the control of the transmitter and receiver sections. For example, when a collision is indicated a node micro-processor is intercepted and a re-transmission procedure is commenced according to a program executed by the micro-processor.

Transmitter in the node.

Inputs to the transmitter 50 are a clock signal, serial non-return-to-zero (NRZ) binary data synchronous with the clock signal, and optionally an enable signal.

The timing reference or clock signal is a symmetrical square wave signal of period T seconds whose positive transitions delimit each serial data bit; i.e. the data signal only changes state on positive transitions of the clock. Thus the clock signal is HIGH for the first half (T/2 seconds) of each data bit period and LOW for the second half.

The serial data signal as constituted by any arbitrary sequence of binary ones and zeros.

As shown in Figure 2 the transmitter comprises two main sections: a ONES section 2,4 and 6, and a ZEROS section 3,5 and 7. The two sections are very similar.

The HIGH level pulse of width T/2 occurs at the

output of gate 2 when the input data is HIGH. This is called a ONES pulse. For the duration of each ONES pulse the line-driver 6 is enabled and drives a signal onto the ONES line of the bus via transformer winding 8a.

The ZEROS section of the transmitter operates in similar fashion when the input data is LOW. Input data passes through inverter 1 to gate 3 where it is combined with the clock signal to form a HIGH level pulse of width T/2 for each ZERO bit in the data. These are called ZEROS pulses, and they enable line-driver 7 which drives the ZEROS line via transformer winding 9a. During the second half of each bit period the ZEROS line is not driven. The polarity in which the line-driver 7 drives the ZEROS line depends on the state of flip-flop 5. This T type flip-flop reverses the output state on the trailing edge of each ZEROS pulse, and thereby causes the sequence of pulses on the ZEROS line to alternate in polarity. This is illustrated in Figure 3. Asynchronous set and reset inputs to flip-flop 5 are driven from the receiver with signals RECEIVED NEGATIVE ZERO and RECEIVED POSITIVE ZERO respectively. These ensure that at the start of a transmission the ZEROS pulse output by the transmitter is opposite in polarity to the last ZEROS pulse appearing on the ZEROS lineine (regardless of the source of the previous transmission).

Receiver in the node.

The receiver 51 shown in Figure 4 comprises three main sections: a ONES section 10, 11, 12 and 13, a ZEROS section 16, 17, 18 and 19, very similar to the ONES section, and an output section 14, 15 and 20 through 25 in which signals recovered in the two preceding sections are processed in various ways to produce the required outputs.

Input signals to the receiver are RECEIVED ONES (a ternary signal coupled from the ONES line by transformer winding 8b), and RECEIVED ZEROS (likewise a ternary signal but coupled from the ZEROS line by transformer winding 9b).

Primary output signals from the receiver are RECEIVED CLOCK, RECEIVED DATA, and COLLISION. Secondary

outputs from the receiver (used by the transmitter) are RECEIVED POSITIVE ONE, RECEIVED NEGATIVE ONE, RECEIVED POSITIVE ZERO, and RECEIVED NEGATIVE ZERO.

In the ONES section, received ONES which may have suffered attenuation and dispersion during transmission over the bus, are first amplified in a limiting differential amplifier 10. The output signal from amplifier 10 is still in basically a ternary form, i.e. alternating positive and negative polarity pulses around a reference level. Output pulses from the amplifier pass to comparator 11 which has balanced threshholds for detecting both positive and negative pulses. The output from comparator 11 changes from LOW to HIGH only when the output of amplifier 10 goes more positive than the positive threshhold, and likewise changes from HIGH to LOW when the output of amplifier 10 goes more negative than the negative threshhold. The output from comparator 11 drives signal edge-detection circuitry 12 which produces a short positive pulse on each transition of its input waveform (both HIGH to LOW and LOW to HIGH transitions). These pulses trigger monostable multivibrator 13 whose monostable period typically is set to a value between 0.3T and 0.5T, where T is the period of one bit time. Thus the signal appearing at the output of multivibrator 13 is a reconstructed binary ONES signal. The output of 13 is combined with the output of comparator 11 in gates 14 and 15 to form the secondary output signals RECEIVED POSITIVE ONE and RECEIVED NEGATIVE ONE which are used by the encoder.

In the ZEROS section received ZEROS are similarly amplified by ampifier 16 and compared with fixed threshholds in comparator 17. The transition of comparator 17 output signal are extracted by edge detection circuit 18 and used to trigger monostable multivibrator 19 which is set to the same period as multivibrator 13. The signal RECEIVED ZEROS at the output of multivibrator 19 is passed to the output section and is also combined with the output of comparator 17 in gates 20 and 21 to form the secondary output signals

RECEIVED POSITIVE ZERO and RECEIVED NEGATIVE ZERO used by the transmitter.

In the output section the binary signals RECEIVED ONES and RECEIVED ZEROS are combined in various ways to produce the required outputs.

In gate 22 RECEIVED ONES and RECEIVED ZEROS are logically OR'ed together to recover the RECEIVED CLOCK signal.

Cross-coupled gates 23 and 24 form a set-reset flip-flop. RECEIVED ONES is the set input, RECEIVED ZEROS the reset input, and RECEIVED DATA is the output.

During a valid transmission, only one of RECEIVED ONES and RECEIVED ZEROS can be HIGH at any instant of time. If both signals are HIGH this condition is detected by gate 25 and signalled as COLLISION.

THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS:

1. A local area network data communications system of the type providing communication between at least a pair of computer devices interfaced with associated communication nodes 52, said nodes including a transceiver 50, 51, wherein said nodes are commonly connected to a pair of communication lines 53, 54, said lines extending throughout the local area network, said lines carrying transmitted signals, each node being adapted to transmit or receive said data to and from said lines.

2. A system as claimed in claim 1 wherein one communication line carries binary one signals and the other line carries binary zero signals.

3. A system as claimed in claim 1 or claim 2 wherein the data comunication links include non-interacting twisted wire pairs, as a pair of co-axial or twin-axial cables.

4. A system as claimed in claim 1, 2 or 3 wherein the communication nodes perform the encoding of binary data into a form suitable for transmitting on the communication lines having equal signal capacity or bandwidth, and the decoding of data received from both lines.

5. A system as claimed in claim 3 wherein the communication lines include a twisted wire pair which are reversable in polarity without affecting the ability of the receiver or transmitter to operate.

6. A system as claimed in claim 2 wherein the communication nodes include means to detect and to signal the existence of simultaneous signal pulses on both lines thereby indicating a collision, and means to retransmit data after a predetermined delay.

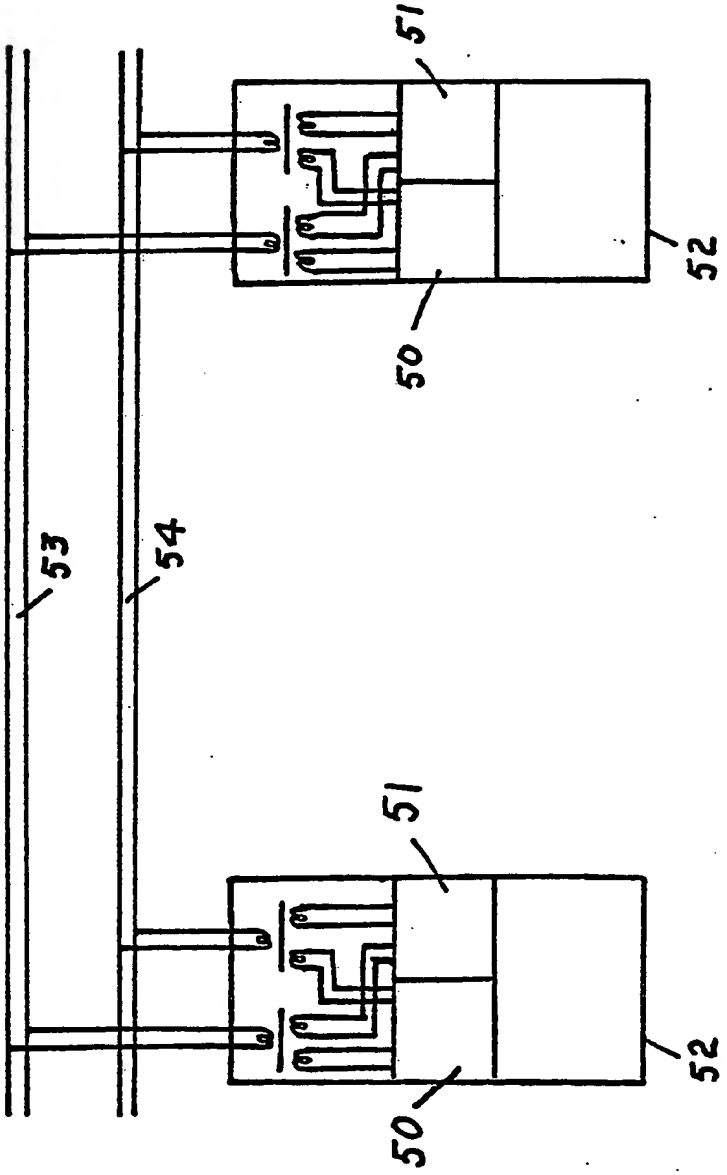

Figure 1

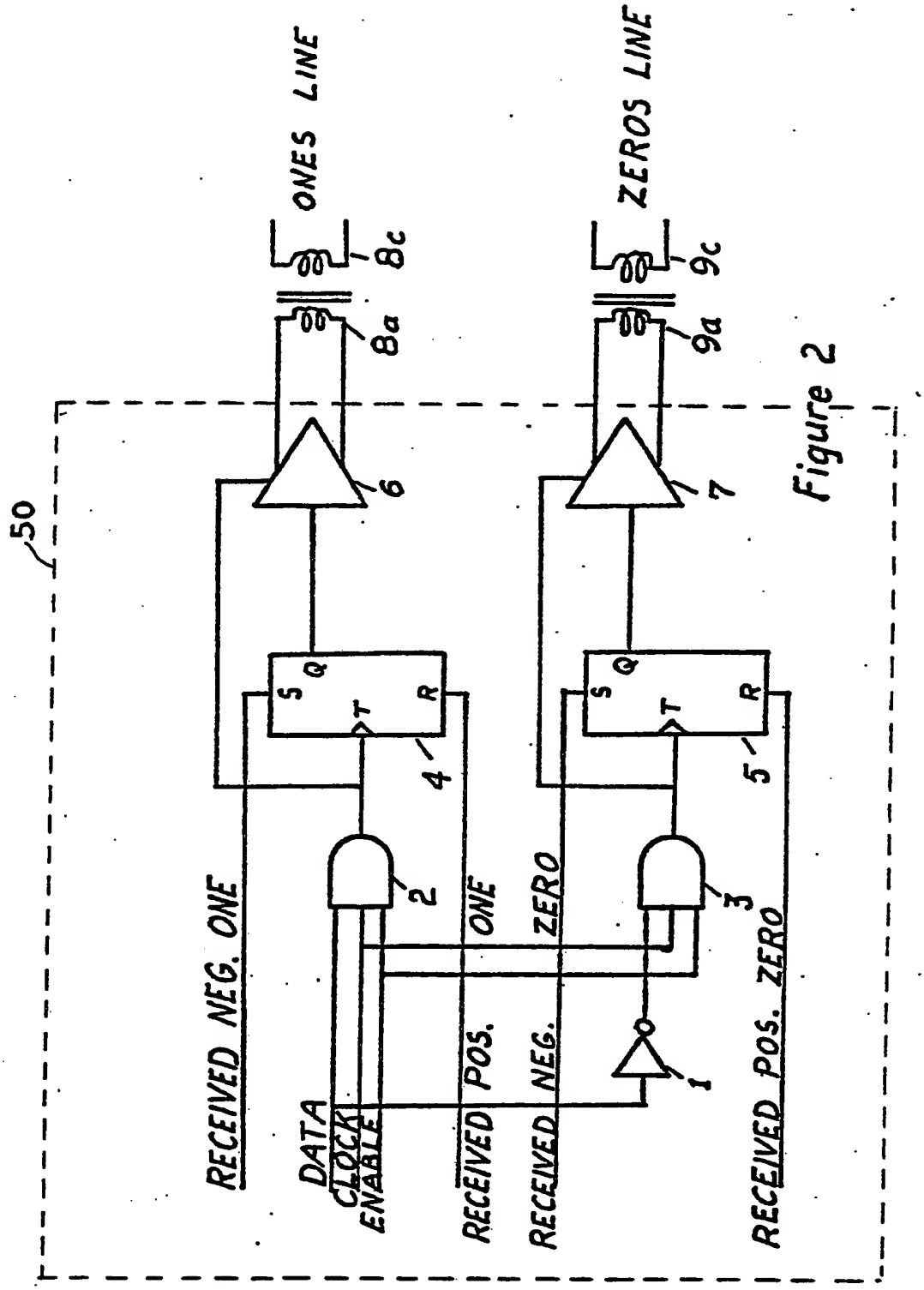

Figure 2

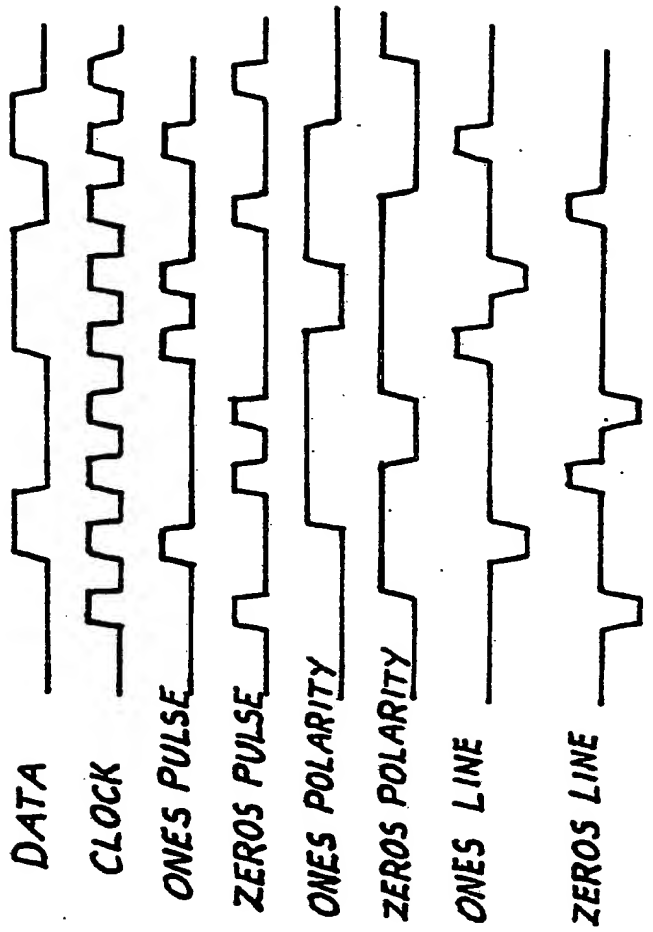

Figure 3

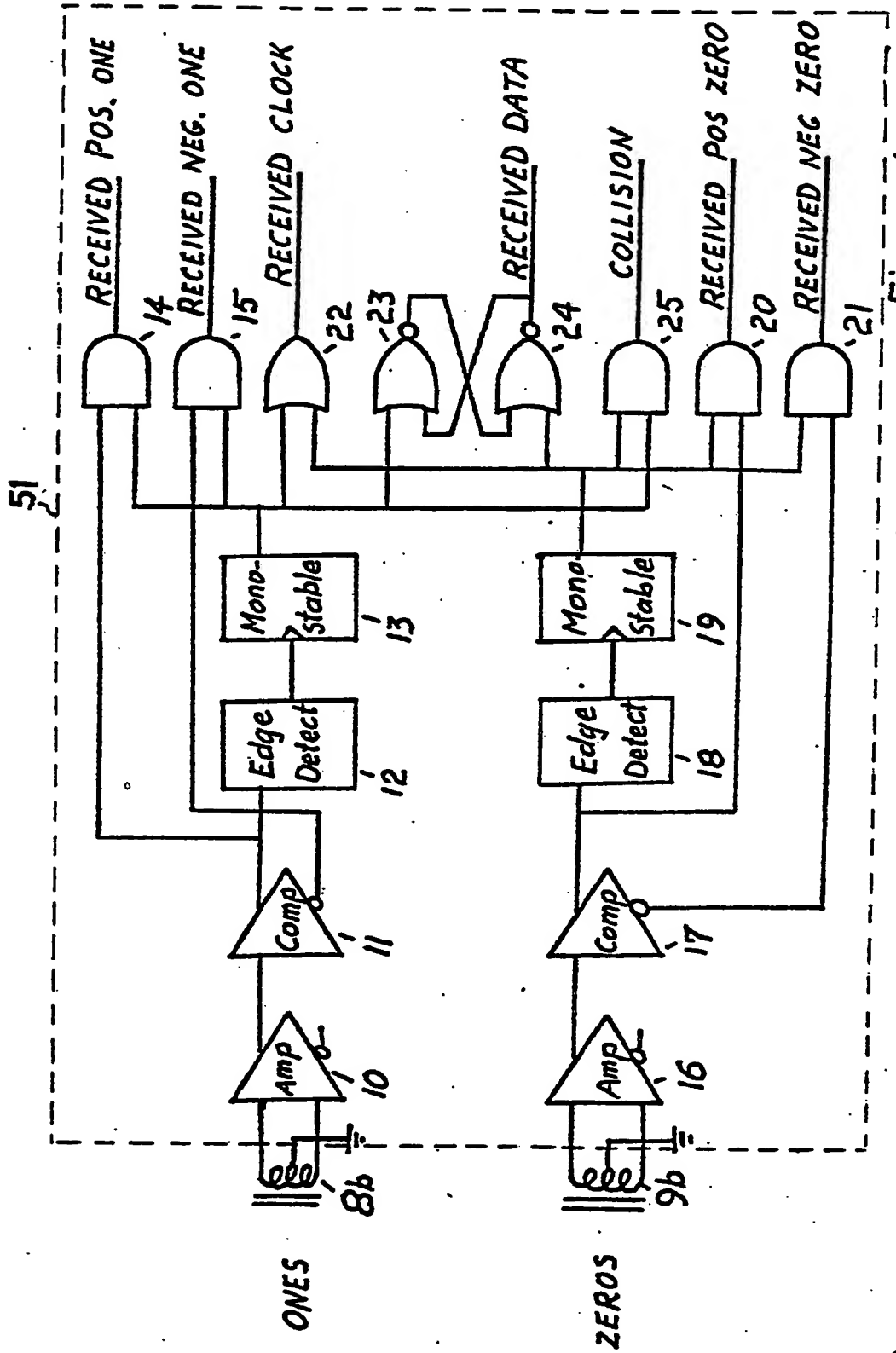

Figure 4.

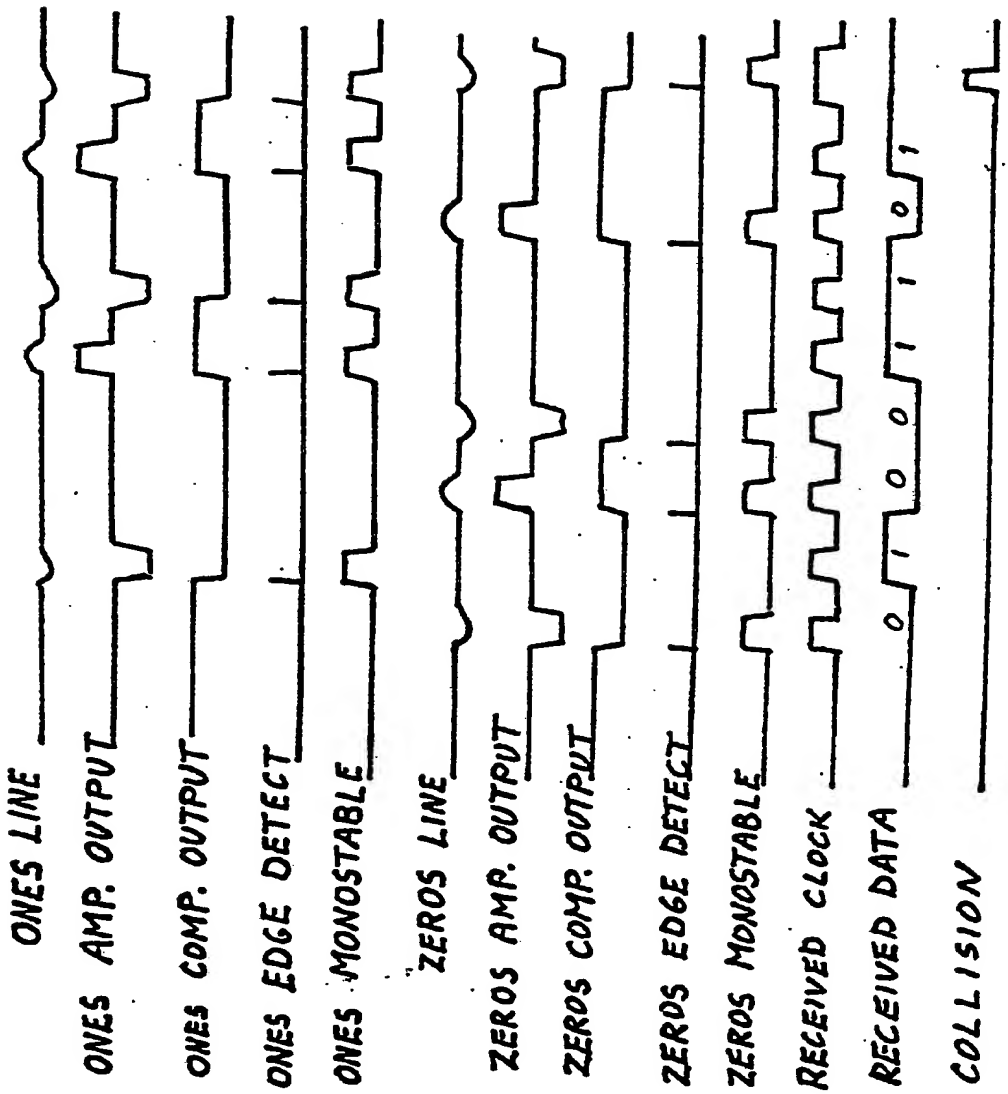

Figure 5.

INTERNATIONAL SEARCH REPORT

International Application No PCT/AU84/00072

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int. Cl.[3] H04L 5/14, G06F 3/04

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
IPC	H04L 5/14, G06F 3/04

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

AU : IPC as above

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
P	EP, A, 0093623 (XEROX CORPORATION) 9 November 1983 (09.11.83) See page 1, line 17 to page 3 line 20; page 5 lines 17-20	(1, 3-6)
P	DE, A, 3142683 (HUBERT) 11 May 1983 (11.05.83)	(1)
P	JP, A, 58-146145 (TOKYO SHIBAURA DENKI KK) 31 August 1983 (31.08.83) (JAPATIC English Language Abstract)	(1)
X,Y	AU, A, 10581/83 (RACAL MILGO LIMITED) 18 August 1983 See page 1A, lines 1-7; page 4, lines 36-38; page 8, line 28 to page 11, line 24. (& GB, A0, 8301920 published 23 February 1983 (23.02.83))	(1, 3-6)
X,Y	AU, A, 84404/82 (AMERICAN STANDARD INC.) 20 January 1983 (20.01.83)	(1,4)
X,Y	US, A, 4320502 (DE VEER) 16 March 1982 (16.03.82) See multiline bus 60, 62 of Fig 4.	(1, 3-5)
X,Y	US, A, 4282512 (BOGGS ET AL) 4 August 1981 (04.08.81) See column 3, lines 14-33	(1, 3-5)
X,Y	US, A, 3886524 (APPELT) 27 May 1975 (27.05.75) See column 1, lines 9-19 Table 1	(1, 3-5)

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IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
28 June 1984 (28.06.84)	(05-07-84) 5, JULY 1984
International Searching Authority [1]	**Signature of Authorized Officer [20]**
AUSTRALIAN PATENT OFFICE	A. S. MOORE A.A. Moore

Form PCT/ISA/210 (second sheet) (October 1981)

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category *	Citation of Document, 16 with indication, where appropriate, of the relevant passages 17	Relevant to Claim No 18
Y	US, A, 4377852 (THOMPSON) 22 March 1983 (22.03.83) See colum 10, lines 64-69	(1)
Y	US, A, 4149238 (JAMES et al) 10 April 1979 (10.04.79)	(1)
Y	GB, B, 1168476 (BRITISH TELECOMMUNICATION RESEARCH LIMITED) 29 October 1979 (29.10.79) See page 1, lines 16-18; page 2, lines 41-45	(1, 3-5)
A	US, A, 4063220 (METCALFE ET AL) 13 December 1977 (13.12.77)	(1,6)
A	US, A, 4099024 (BOGGS ET AL) 4 July 1978 (04.07.78)	(1,6)

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON
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Patent Document Cited in Search Report	Patent Family Members		
AU 10581/83	DK 435/83	EP 86577	FI 830415
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AU 84404/82	BR 8203678		
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	ES 477456	FR 2418494	GB 2015217
	JP 54112105	JP 58044561	SE 7901517
US 4282512	CA 1160308	EP 33665	EP 87664
	JP 56122549		
US 3886524	DE 2448212	FR 2248554	GB 1487953
	JP 50068626		
US 4149238	CA 1095604		

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INTERNATIONAL APPLICATION NO. PCT/AU PCT/AU84/00072 (CONTINUED)

Patent Document Cited in Search Report	Patent Family Members
GB 1168476	DE 1512140, NL 6706828, US 3680053
US 4063220	CA 1056510, CH 615286, DE 2557896, FR 2306478, GB 1517566, IT 1052088, JP 51114804, NL 7515217, SE 7514708

END OF ANNEX